REMARKS/ARGUMENTS

In the Office Action, the Examiner noted that claims 1-23 are pending in the application. The Examiner additionally stated that claims 1-23 are rejected. By this amendment, claims 1-2, 9-10, 13-14, and 21-23 have been amended. Hence, claims 1-23 are pending in the application.

Applicant hereby requests further examination and reconsideration of the application, in view of the foregoing amendments.

In the Specification

The Examiner objected to the specification 1) because the headings of each section should not be underlined or in boldface type as described in 37 CFR 1.77(c); and 2) because of the following informality: page 1 of the specification has missing application numbers, which must be filled in.

Applicant has amended the specification to provide normal font section headings instead of boldface font section headings. In addition, Applicant has amended the section entitled CROSS REFERENCE TO RELATED APPLICATIONS to fill in the missing application numbers. Accordingly, Applicant respectfully requests that the Examiner withdraw his objections to the specification.

Applicant has furthermore amended the specification to secure a substantial correspondence between the claims amended herein and the remainder of the specification. No new matter is presented.

In the Claims

Claim Objections

The Examiner objected to the claims because of several informalities, all of which have been addressed by amendments to the claims. Applicant particularly notes the Examiner's comment that misnumbered claim 22 has been renumbered 23, and herein makes reference to renumbered claim 23. Accordingly, Applicant respectfully requests that the Examiner withdraw his objections to the claims.

Rejections Under 35 U.S.C. §103

The Examiner rejected claims 1-8 and 22 under 35 U.S.C. 102(a) as being unpatentable over Moyer (5,983,338) in view of Strongin (6,559,850 B1). Applicant respectfully traverses the Examiner's rejections.

With regard to claim 1, the Examiner noted that Moyer has disclosed an interface (figure 1, element 30) for transferring data between a central processing unit (CPU) (figure 1, element 12) and a plurality of coprocessors (figure 1, elements 14 and 16), the interface comprising:

i. an instruction bus (column 6, line 34 and figures 2 and 3, element 61), configured to transfer instructions to a plurality of coprocessors in an instruction transfer order (an order is inherent), wherein particular instructions direct designated ones of the plurality of coprocessors to transfer data to/from the CPU (figures 22-26, UU field); and

ii. a data bus (column 8, lines 65-66 and figures 2 and 3, element 72), coupled to said instruction bus (since both go from processor to coprocessor, they are coupled), configured to subsequently transfer the data.

The Examiner furthermore stated that Moyer does not disclose wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, but that Strongin has disclosed in figures 3 and 4 a read retrieval order that differs from the read request order. The Examiner noted that an instruction as in Moyer is essentially a request for data or a read request. When the data is sent, that is a read retrieval. The Examiner remarked that the figure shows signals (identifier) that indicate the order of the data, and that Strongin has shown in column 6, lines 36-44 that this difference in ordering allows for data accesses to be quicker, and thus, the quickness of data access would have motivated one of ordinary skill in the art to modify the design of Moyer to include the out of order data retrieval disclosed by Strongin. The Examiner concluded that it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the design of Moyer to retrieve data out of order as taught by Strongin so that data accesses can be achieved quicker.

Claim 1 as amended is provided below for ease of reference.

1. An interface for transferring data between a central processing unit (CPU) and a plurality of coprocessors, the interface comprising:

an instruction bus, configured to transfer instructions to the plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU; and

a data bus, coupled to said instruction bus, configured to subsequently transfer the data, wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

In combination, claim 1 recites an instruction bus and a data bus that provide an interface for transferring data between a CPU and a plurality of coprocessors. The instruction bus transfers instructions to the plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer the data to/from the CPU. The data bus subsequently transfers the data in a data transfer order that differs from the instruction transfer order. Data order signals within the data bus prescribe the data transfer order such that transfer of a data element corresponding to a specific outstanding instruction is prescribed relative to all outstanding instructions.

Applicant has studied the teachings of both Moyer and Strongin and finds that both teach the transfer of data to/from a coprocessor (or, in the case of Strongin, the transfer of read requests to an AGP-enabled Northbridge). Moyer teaches in order data transfer. Strongin teaches out of order data transfer where a transaction ID is associated with each individual data transaction. Figures 3-8 and associated description in Strongin teaches that each transaction ID is associated with individual data transactions within a number of AGP pipelined transactions, to identify the individual transactions. The association of a transaction ID with the individual transactions included associating a transaction ID with

each individual read request within a number of AGP pipelined read requests and associating *an identical* transaction ID with each individual data unit, within a number of pipelined data units, corresponding to each individual memory request within the numbr of AGP pipelined memory requests. (Abstract)

Applicant's invention, on the other hand, provides for data order signals within a data bus that prescribe a data transfer order that differs from an instruction transfer order, and moreover that the data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction *relative to all outstanding instructions*. Applicant has searched the teachings of both Moyer and Strongin and finds that neither of the inventors, separately or in combination, provide any motivation whatsoever to one skilled in the art to provide apparatus or method having data order signals that prescribe transfer of a data element corresponding to a specific outstanding instruction *relative to all outstanding instructions*. Applicant moreover notes that Strongin teaches away from prescribing transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions by noting "since the transaction ids 3001-300N are to be denoted by the use of 3 data lines, or 3 bits, the greatest number of transaction ids that can be established is 8." (col. 12, lines 5-8) In summary, Strongin teaches assignment of a transaction ID to a data element that is identically fixed to a corresponding AGP read request. In contrast, Applicant's invention claims data order signals that prescribe transfer of a data element corresponding to a specific outstanding instruction *relative to all outstanding instructions*.

In summary then, neither, Moyer nor Strongin provide any teaching or motivation that would lead one skilled in the art to provide for data order signals that prescribe transfer of a data element corresponding to a specific outstanding instruction *relative to all outstanding instructions*. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejection of claim 1.

With respect to claims 2-8, these claims depend from claim 1 and add further limitations that are neither anticipated nor made obvious by Moyer, Strongin, or Moyer and Strongin

in combination. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections to claims 2-8.

Claim 22 is provided below for ease of reference.

22. A method for transferring data between a CPU and a plurality of coprocessors, the method comprising:

transmitting instructions to the plurality coprocessors, each of the instructions directing a data transfer between the CPU and a specific coprocessor, wherein said transmitting is provided in a specific instruction order;

subsequently transferring the data in an order different from the specific instruction order, said transferring comprising:

prescribing transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions, the outstanding instructions being those instructions that have not completed a subsequent data transfer.

In arguments drawn from the same points as made with reference to the rejection of claim 1, the Examiner provided his reasons for rejecting claim 22. In response, Applicant asserts that claim 22 recites, in combination with other method elements "prescribing transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions, the outstanding instructions being those instructions that have not completed a subsequent data transfer." The "relative to all outstanding instructions" limitation, which is similar to apparatus elements of claim 1, is neither taught nor suggested by Moyer, Strongin, or Moyer and Strongin in combination. Applicant therefore respectfully asks that the rejection of claim 22 be withdrawn.

The Examiner rejected claims 9 and 23 under 35 USC 103(a) as being unpatentable over Moyer in view of Strongin as applied to claims 1-8 and 22, and further in view of Hennessy. Applicant respectfully traverses. And in that Applicant has argued over the combination of Moyer's and Strongin's teachings with reference to the rejections of claims 1 and 22, and noting that claim 9 depends from claim 1 and adds further

limitations, it is respectfully requested that the Examiner withdraw his rejection of claim 9. Likewise, since claim 23 depends from claim 22 and adds further limitations, Applicant respectfully requests the withdrawal of the rejection of claim 23.

The Examiner rejected claims 10-12 and 14-20 under 35 USC 103(a) as being unpatentable over Moyer in view of Tanenbaum and further in view of Strongin. Applicant respectfully traverses the Examiner's rejections.

With regard to claim 10, the Examiner stated that Moyer discloses a computer program product for use with a computing device, the computer program product comprising:

> i. a computer usable medium, for causing a coprocessor interface to be described that transfers data between a CPU and a plurality of coprocessors, said computer readable program code comprising:
>
> > (1) an instruction bus, said instruction bus configured to transfer instructions to said plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer said data to/from said CPU; and
> >
> > (2) a data bus, said data bus configured to subsequently transfer said data.

The Examiner remarked that Moyer does not disclose having computer readable program code embodied in said medium and first program code and second program code. The Examiner added that Moyer does not disclose wherein said data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order. The Examiner stated that Tanenbaum has disclosed on pages 10-12 that hardware is logically equivalent to software and that the boundaries between them are fluid, noting that Strongin has disclosed in figures 3 and 4 a read retrieval order that differs from the read request order. The Examiner stated that an instruction in Moyer is essentially a request for data or a read request. When the data is sent, that is a read retrieval. The Examiner remarked that the figure shows signals (identifier) that indicate the order of the data.

In addition, the Examiner noted that Tanenbaum has shown on page 11 that for one factor involved in deciding whether to implement a function in hardware or software is frequency of change, stating that it is easier to change software code than to change the layout of a hardware system. The Examiner remarked that this ease of change would have motivated one of ordinary skill in the art to modify the design of Moyer to implement the disclosed apparatus as program code taught by Tanenbaum. It was noted that Strongin has shown in column 6, lines 36-44 that this difference in ordering allows for data accesses to be quicker, and that this quickness of data access would have motivated one of ordinary skill in the art to modify the design of Moyer to include the out of order data retrieval disclosed by Strongin.

The Examiner concluded that it would have be obvious to one of ordinary skill in the art at the time of the invention to modify the design of Moyer to implement his design in program code as taught by Tanenbaum and to retrieve data out of order as taught by Strongin so that data accesses can be achieved quicker and so that changes may be made easier.

Claim 10 is provided below for ease of reference.

10. A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a coprocessor interface to be described that transfers data between CPU and a plurality of coprocessors, said computer readable program code comprising:

first program code, for providing an instruction bus, said instruction bus configured to transfer instructions to said plurality of coprocessors in an instruction transfer order, wherein particular instructions direct designated ones of the plurality of coprocessors to transfer said data to/from said CPU; and

second program code, for providing a data bus, said data bus configured to subsequently transfer said data, wherein data order signals within said data bus prescribe a data transfer order that is different from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

In transversal of the Examiner's rejection of claim 10, Applicant responds that claim recites, in combination with other elements "second program code, . . . , wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions." This limitation, similar to that recited in claim 1, and similar to the method element recited in claim 22, is neither taught nor suggested by Moyer, Strongin, or Moyer and Strongin in combination. Furthermore, although Tanenbaum may suggest that hardware is logically equivalent to software and that the boundaries between hardware and software are fluid, a motivation to implement, in program code rather than hardware, data order signals that prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions, is absent apart from a motivation or other suggestion to do so in hardware. Accordingly, Applicant respectfully requests that the rejection of claim 10 be withdrawn.

With regard to claims 11-12, these claims depend from claim 10 and add further limitations that are neither anticipated nor made obvious by Moyer, Strongin, Tanenbaum, or any combination of the three aforementioned references. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections of claims 11-12.

Claim 14 is provided below for ease of reference.

14. A computer data signal embodied in a transmission medium, the computer data signal comprising:

computer-readable first program code, for providing an instruction bus for transferring instructions to a plurality of coprocessors in an instruction transfer order, wherein particular instructions direct particular coprocessors to transfer data to/from a CPU; and

computer-readable second program code, for providing a data bus for subsequently transferring said data, wherein data order signals within said data bus prescribe a data transfer order that differs from said instruction transfer order, and wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions.

In arguments drawn from the same points as made with reference to the rejection of claim 10, the Examiner provided his reasons for rejecting claim 14. In response, Applicant asserts that claim 14 recites, in combination with other elements, "computer-readable second program code, . . . wherein said data order signals prescribe transfer of a data element corresponding to a specific outstanding instruction relative to all outstanding instructions." This limitation, similar to the limitations discussed above in traversal of the rejection of claim 10, are neither taught nor suggested by Moyer, Strongin, Tanenbaum, or any combination of the three references. Applicant therefore respectfully asks that the rejection of claim 14 be withdrawn.

With regard to claims 15-20, these claims depend from claim 14 and add further limitations that are neither anticipated nor made obvious by Moyer, Strongin, Tanenbaum, or any combination of the three aforementioned references. Accordingly, Applicant respectfully requests that the Examiner withdraw his rejections of claims 15-20.

The Examiner rejected dependent claims 13 and 21 under 35 USC 103(a) as being unpatentable over Moyer in view of Tanenbaum and further in view of Strongin as applied to claims 10-12 above, and further in view of Hennessy. Applicant respectfully traverses and directs the Examiner's attention to arguments made in traversal to the rejections of independent claims 10 and 14. Consequently, in that claim 13 depends from

claim 10 and in that claim 21 depends from claim 14, and in that these claims add further limitations that are neither anticipated nor made obvious by Moyer, Strongin, Hennessy, Tanenbaum, or any combination of the four aforementioned references, Applicant respectfully asks that the rejections of claims 13 and 21 be withdrawn.

In the Drawings

The Examiner objected to the drawings as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: element 316 of figure 3 and element 800 of figure 8 are not mentioned in the specification. The Examiner required a proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, in reply to the Office Action to avoid abandonment of the application. Also, the Examiner objected to the drawings under 37 CFR 1.83(a), noting that they must show every feature of the invention specified in the claims. In particular, the Examiner stated that the 3-D graphics accelerators must be shown or the feature(s) cancelled from the claims.

Applicant respectfully notes that element 316 is mentioned in the description on page 22, line 20. In addition, Applicant has amended the specification to include element 800 of figure 8. Also, Applicant has amended claim 2 to recite "graphics (3-D) coprocessors" instead of "3-D graphics accelerators." The specification notes that a graphics (3-D) coprocessor is one type of a coprocessor that is comprehended by the present invention.

Accordingly, it is therefore requested that the Examiner withdraw his objections to the drawings.

CONCLUSIONS

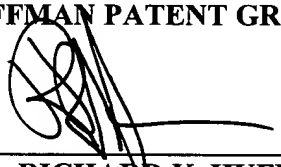
In view of the arguments advanced above, Applicant respectfully submits that claims 1-23 are in condition for allowance. Reconsideration of the rejections is requested, and allowance of the claims is solicited.

Applicant earnestly requests that the Examiner contact the undersigned practitioner by telephone if the Examiner has any questions or suggestions concerning this amendment, the application, or allowance of any claims thereof.

EXPRESS MAIL LABEL NUMBER: **EO 001 699 884 US**
DATE OF DEPOSIT: **4/9/2004**
I hereby certify that this paper is being deposited with the U.S. Postal Service Express Mail Post Office to Addressee Service under 37 C.F.R. §1.10 on the date shown above and is addressed to Mail Stop PETITION, Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

Respectfully submitted,

HUFFMAN PATENT GROUP, LLC



By _____

RICHARD K. HUFFMAN
Reg. No. 41,082
Tel.: (719) 575-9998